Nayan Vyas Career Objective 

Bachelor of Engineering (EleI am a VLSI enthusiast currently seeking Design & Verification Roles in the

industry. Being a 2021 graduate, I am familiar with the recent

advancements in Semiconductor space. I want to grow as a professional

VLSI Engineer and contribute my knowledge and skills to the organization I

am working for.

Work Experience

Personal details

Associate Engineer - Firmware Engineering DSP

Vertiv Energy Private Limited, Pune

Sep 2021 - Jan 2023

Name

Nayan Vyas

Email address

nayanvyas09@gmail.com Phone number

Responsible for Firmware Development of Industrial & Commercial grade UPS ranging from 120 kVA to 1200 kVA

Developed & modified Firmware for Texas Instruments DSP for clients like TSMC , Microsoft, etc.

Professional Training

+918226031065

Address

Pune, Maharshtra

LinkedIn

linkedin.com/in/nayan-vyas vlsi-engineer

Achievements

Advanced VLSI Design & Verification Course

Maven Silicon VLSI Training Institute,, Bangalore Education

ctronics & Telecommunication)

Savitribai Phule Pune University

May 2022 - Present Aug 2017 - Aug 2021

Was Awarded Star of the Month, September 2022 - Maven Silicon

Was elected as "Cultural Representative" at Bharati Electronics & Telecommunication Association(BETA) in college.

Founder & active

member of Musical Society -"Tarang" during college.

Was elected as “Head Boy” in school

Secured 1st position for consecutive 12 yrs

throughout the school.

12th Standard May 2016 - May 2017 Nirmala Convent Sr. Sec. School Ujjain

10th Standard May 2014 - May 2015 Nirmala Convent Sr. Sec. School Ujjain

Projects

Router 1x3 – RTL Design and Verification

The router accepts data packets on a single 8-bit port and routes them to one of the three output channels, channel0, channel1 and channel2. Architected the block level structure for the design

Implemented RTL using Verilog HDL.

Architected the class based verification environment using System Verilog.

Verified the RTL model using System Verilog. Generated functional and code coverage for the RTL verification sign-off.

Synthesized the design.

Smart Toilet Using PIR Sensor For

Railways

The project deals with a PIR sensor controlled Railway Toilet which does multiple operations based on the input received by the sensor. Implemented Atmega328P microcontroller based design(Bare

Hobbies

Singing

Poetry

Films

Adventure

Behavioural Skills

Self Awareness

Optimism

Quick decision making Calm Attitude

minimum Arduino).

Power efficient & Cost effective design .

Advancement over currently installed error prone mechanical system. Skills

VLSI Domain Skills -

HDL: Verilog

HVL: System Verilog

Verification Methodologies: Constraint Random Coverage Driven Verification, Assertion Based Verification - SVATB

Methodology: UVM

Protocols: AXI, AHB, UART, I2C, SPI

EDA Tool: Mentor Graphics - Questasim

Domain: ASIC/FPGA front-end Design and Verification

Operating System: Linux

Scripting Languages: Perl Scripting

Core Skills: RTL Coding using Synthesizable constructs of Verilog, FSM based design, Simulation, CMOS Fundamentals, Code Coverage, Functional Coverage, Synthesis, Static Timing Analysis(STA), Solid State Electronics.

Programming Skills -

C [Pointers | Memory Allocation | Data structure, etc.]

C++ ( Good knowledge of OOPs concept, Class, Inheritance, Polymorphism etc.)

Embedded C

Other Skills -

Firmware Development, CAN protocol, Code

Composer Studio(CCS), PCB Design, Proteus.

Workshops/Certifications

1. "Machine Learning" Online Training by Analytics Vidhya(Internshala).

2. "Industrial IOT & Artificial Intelligence" Certification Course by Innovura Academy, Pune.

3. "Robotics: Bluetooth Operated Line Follower Bot " Hands-On Certification Course by SSIGMA.

Declaration

2020 2019

2018

I here by declare that the above mentioned information is correct to the best of my knowledge and I bear the responsibility for the correctness of the same.

Date :

Place: Nayan Vyas